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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/775,232

02/11/2004

Norio Takahashi

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EXAMINER

PATEL, ISHWARBHAI B

ART UNIT

PAPER NUMBER

2841

DATE MAILED: 01/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/775,232

Applicant(s)

TAKAHASHI, NORIO

Examiner

Ishwar (I. B.) Patel

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 February 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 6,7 and 13-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 6,7 and 13-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 09/450,504.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 2/11/04 & 9/15/04.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Divisional

1. This application is a divisional of application 10/289,358 filed on November 7, 2002. The examiner has reviewed the prior art used in the parent application.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 09/450,504, filed on November 30, 1999.

Claim Objections

4. Claim 13 objected to because of the following informalities: In claim 13, "trances" line 2, should be trenches. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claim 6 is rejected under 35 U.S.C. 102(b) as being anticipated by Yasuhiro (Japanese Patent No. JP402113596A).

Regarding claim 6, Yasuhiro, in figure 1, discloses a circuit board for a semiconductor device comprising: a plurality of pads (2, on left of figure 1) on which the semiconductor device is to be mounted, said pads being formed on the circuit board (4), and said pads being disposed in a first line (see figure 1, only cross section is shown); a plurality of terminals (2, on the right side of the figure) formed on a side edge of the circuit board, said terminals being disposed in a second line (see figure 1, only cross section is shown); which is in parallel to said first line of said pads (see figure 1); a resist film (3) covering an area on the circuit board between said pads and said terminals; and a barrier formed between said first line of said pads and said second line of said terminals, said barrier including a plurality of trench (plurality of trenches between the pad on the left and the pad 2 on the right side of figure) disposed along said terminals, and said trenches being formed in said resist film

7. Claim 6 is rejected under 35 U.S.C. 102(a) as being anticipated by Japanese Application Number 1998JP-0137329 (JP329).

Regarding claim 6, JP329, in figure 1, discloses a circuit board for a semiconductor device comprising: a plurality of pads (6, on the left of the figure) on which the semiconductor device is to be mounted, said pads being formed on the circuit board (1), and said pads being disposed in a first line (see figure 1, only cross section is shown); a plurality of terminals (2C, on the right of the figure) formed on a side edge of the circuit board, said terminals being disposed in a second line, which is in parallel to said first line of said pads (see figure 1, only cross section is shown); a resist film (3) covering an area on the circuit board between said pads and said terminals; and a barrier formed between said first line of said pads and said second line of said terminals, said barrier including a plurality of trench (plurality of trenches formed between the pad 6 on the left of the figure and terminal 2, on the right side of the figure 1) disposed along said terminals, and said trenches being formed in said resist film (see figure).

8. Claims 6 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Suzuki (US Patent No. 5,925,445).

Regarding claim 6, Suzuki, in figure 3, discloses a circuit board for a semiconductor device comprising: a plurality of pads (2, on the left of the figure) on which the semiconductor device is to be mounted, said pads being formed on the circuit board (1), and said pads being disposed in a first line (see figure); a plurality of terminals (7, on the right side of figure) formed on a side edge of the circuit board, said terminals being disposed in a second line (see figure), which is in parallel to said first

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line of said pads (see figure); a resist film (4b, 4c) covering an area on the circuit board between said pads and said terminals; and a barrier formed between said first line of said pads and said second line of said terminals, said barrier including a plurality of trench (plurality of trenches formed between the pad 2 on the left of the figure and the terminals 7 on the right side of figure) disposed along said terminals, and said trenches being formed in said resist film (see figure).

Regarding claim 7, Suzuki further discloses said trenches are parallel to each other (see figure).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claims 13-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki as applied to claim 6 above.

Regarding claim 13, Suzuki discloses all the features of the claimed invention including the trenches as applied to claim 6 above, but does not disclose a distance between trenches is 1 mm. However, as can be seen from the figure the distance between the trenches will depend upon the size of the pad required as the pads are exposed between the resist. The pad size will depend upon the interconnection

structure with the corresponding interconnect to be connected to have reliable interconnection. Further, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the structure of Suzuki with a distance between trenches as 1 mm, in order to have desired width of the pad to have a reliable interconnection.

Regarding claim 14, the modified structure of Suzuki discloses said terminals are disposed in a certain length, which is shorter than a length of said barrier (see figure).

Regarding claim 15, the modified structure of Suzuki discloses a depth of the barrier equals the thickness of the resist film (see figure).

Regarding claim 16, the modified structure of Suzuki discloses all the features of the claimed invention including the trench had a width of 1 mm, as applied to claim 13 above.

Regarding claim 17, the modified structure of Suzuki discloses said terminals are disposed in a certain length, which is shorter than a length of said barrier (see figure).

Regarding claim 18, the modified structure of Suzuki discloses a depth of the barrier equals the thickness of the resist film (see figure).

Regarding claim 19, the modified structure of Suzuki discloses each trench had a width of 1 mm as applied to claim 16 above.

Regarding claim 20, the modified structure of Suzuki discloses said terminals are disposed in a certain length, which is shorter than a length of said barrier (see figure).

Regarding claim 21, the modified structure of Suzuki discloses a depth of the barrier equals the thickness of the resist film (see figure).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Moriyama (US Patent No. 6,143,991), in figure 3B, discloses a solder resist between the bump electrode (3,4) and the internal wiring pad 2.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Ishwar (I. B.) Patel
Examiner
Art Unit: 2841
January 8, 2006